SC4000™
Universal Timeslot Interchange

VLSI
Technology

OVERVIEW

The SC4000 Universal Timeslot Interchange is an integrated circuit which provides a high bandwidth interface to several industry standard expansion buses used in telecommunications and telephony systems. The device is fully software programmable, and can be controlled by a wide variety of microprocessors. The SC4000 provides timeslot interchange between multiple serial TDM streams on a local bus and an expansion bus. Internal buffering allows the exchange of timeslots between local and expansion buses with different speeds and architectures. On the local bus side, the SC4000 outputs and accepts data from either four serial data streams at 2.048 Mbps, or two streams at 4.096 Mbps, or one stream at 8.192 Mbps.

On the expansion bus side, it outputs and accepts data from sixteen serial data streams operating at either 2.048, 4.096, or 8.192 Mbps.

The SC4000 has a non-blocking switching capacity of 128 x 2048 bi-directional DS0 (64 Kbps) timeslots. It is designed for connecting multiple telephony interfaces or signal processing resources to an expansion bus. Since the device supports timeslot bundling, it is optimal for interfacing higher bandwidth media streams.

The SC4000 can be programmed to receive or transmit timeslot data in parallel format through the micro-processor interface. The SC4000 can also switch data between local bus timeslots without accessing or using bandwidth on the expansion bus.

The SC4000 supports two different expansion bus architectures, SCbus™

(SCSA™) and MVIP Bus (MVIP-90™). It is also compatible on the local bus side with ST-Bus, GCI and PEB conventional bus formats. This multi-mode capability enables designers to build a single product or platform which can be implemented in different system architectures or operated in different compatibility modes.

SCbus is a high speed serial TDM bus designed for connecting devices in telecommunications and computer systems. It supports up to 2048 bi-directional time slots, clocking, and an optional HDLC messaging channel which can be used for signaling. SCbus can be implemented as a mezzanine bus for PC platforms and as a VME I/O bus. SCbus has been endorsed by VITA (VMEbus Industry Trade Association) and ANSI (American National Standards Institute).
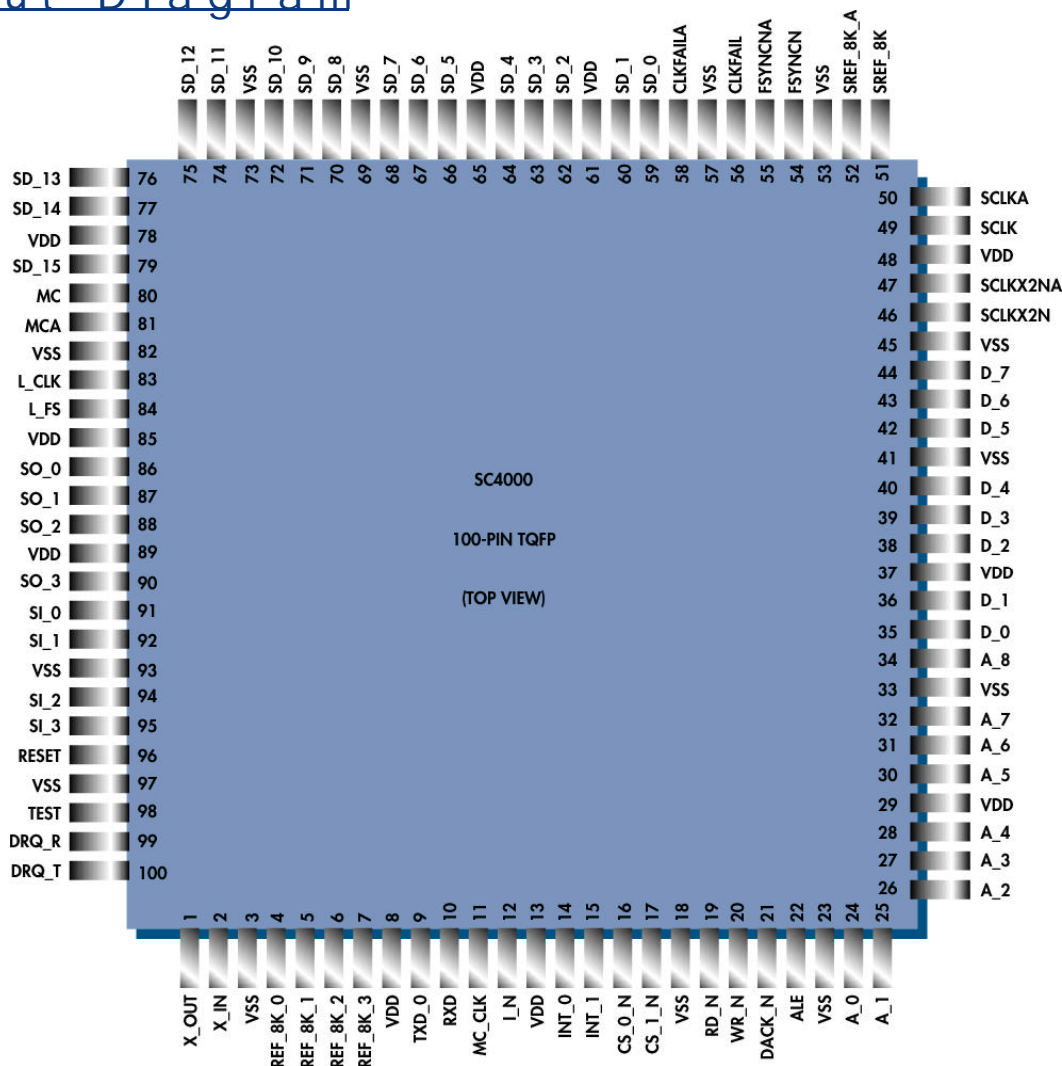
Block Diagram
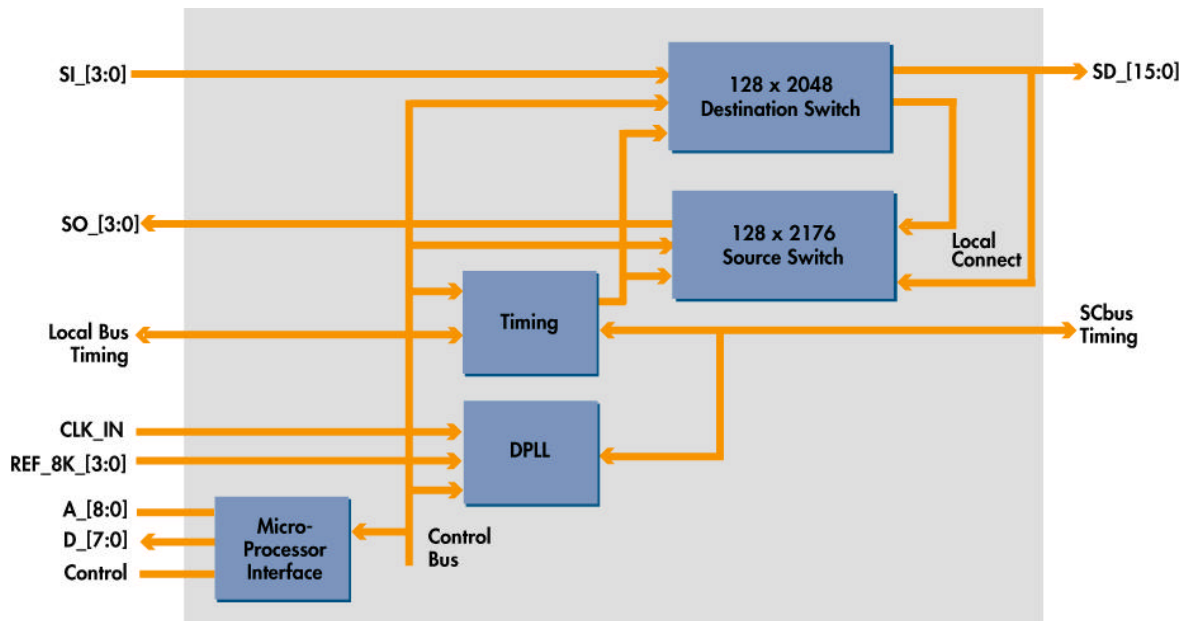
MVIP Bus is a multiplexed TDM bus designed to carry telephone traffic between circuit boards within a PC. It supports up to 256 full-duplex channels and clocking, and is implemented on a ribbon cable. It is endorsed by GO-MVIP, Inc.

FEATURES

- Timeslot interchange between local / expansion buses
- Multiple expansion bus formats:
  · SCbus, MVIP
- Multiple local bus speeds and formats:
  · 2.048, 4.096 or 8.192 Mb/s
  · PEB, ST bus or GCI
- Controllable with multiple microprocessor types
- Serial or parallel access to expansion bus
- Internal phased lock loop
- Fast response clock fallback
- Flexible local frame sync interface
- SCbus message bus interface
- High availability and self-diagnostic features
- 5 V CMOS technology
- 100-pin TQFP package
- Full switching between any of:
  · 128 local bus input timeslots
  · 128 local bus output timeslots
  · Up to 2048 expansion bus timeslots

Pinout Diagram

SC4000
100-PIN TQFP
(TOP VIEW)

Left side (top to bottom): SD_13 (76), SD_14 (77), VDD (78), SD_15 (79), MC (80), MCA (81), VSS (82), L_CLK (83), L_FS (84), VDD (85), SO_0 (86), SO_1 (87), SO_2 (88), VDD (89), SO_3 (90), SI_0 (91), SI_1 (92), VSS (93), SI_2 (94), SI_3 (95), RESET (96), VSS (97), TEST (98), DRQ_R (99), DRQ_T (100)

Top side (left to right): SD_12 (75), SD_11 (74), VSS (73), SD_10 (72), SD_9 (71), SD_8 (70), VSS (69), SD_7 (68), SD_6 (67), SD_5 (66), VDD (65), SD_4 (64), SD_3 (63), SD_2 (62), VDD (61), SD_1 (60), SD_0 (59), CLKFAILA (58), VSS (57), CLKFAIL (56), FSYNCNA (55), FSYNCN (54), VSS (53), SREF_8K_A (52), SREF_8K (51)

Right side (top to bottom): SCLKA (50), SCLK (49), VDD (48), SCLKX2NA (47), SCLKX2N (46), VSS (45), D_7 (44), D_6 (43), D_5 (42), VSS (41), D_4 (40), D_3 (39), D_2 (38), VDD (37), D_1 (36), D_0 (35), A_8 (34), VSS (33), A_7 (32), A_6 (31), A_5 (30), VDD (29), A_4 (28), A_3 (27), A_2 (26)

Bottom side (left to right): X_OUT (1), X_IN (2), VSS (3), REF_8K_0 (4), REF_8K_1 (5), REF_8K_2 (6), REF_8K_3 (7), VDD (8), TXD_0 (9), RXD (10), MC_CLK (11), I_N (12), VDD (13), INT_0 (14), INT_1 (15), CS_0_N (16), CS_1_N (17), VSS (18), RD_N (19), WR_N (20), DACK_N (21), ALE (22), VSS (23), A_0 (24), A_1 (25)

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